Features and Benefits

- Digital output X-, Y-, and Z-Axis angular rate sensors(gyros) on the integrated circuit
- Three integrated 11-bit ADCs provide simultaneous sampling of gyros while requiring no external multiplexer
- Enhanced bias and sensitivity temperature stability reduces the need for user calibration
- Improved Low frequency noise performance
- Low 6mA operating current consumption for long battery life
- Wide VDD supply voltage range of 2.1V to 5V
- Standby current: 5 μ A
- Small and thin package for portable devices
- 4x4x1.2mm^3 QFN
- No high pass filter needed
- Factory calibrated scale factor
- Fast Mode IIC (400KHz) serial interface
- SPI interface
- 2000º/s factory set full scale range
- On chip EPROM trimming
- Small footprint with horizontal mounting
- Operating temp range:- 40℃ to 85℃
- Digital programmable low-pass filter
- FIFO buffers the complete data set

General Description

The ST200GC is a single-chip embedded tri-axis MEMS angular rate sensor with an auxiliary IiC interface to third party digital accelerometers, and it is capable of delivering a completed 6-axis sensor raw data via its IIC interface.

The ST200GC features three 11-bit analog-to-digital converters for digitizing outputs. A single QFN package contains high performance micro-machined silicon sensor with signal conditioning circuitry. It provides excellent temperature stability and good resolution over the operating temperature range (-40℃~85℃).

The ST200GC includes programmable digital low-pass filters and EPROM for on-chip sensor factory calibration. Factory trimmed scale factors eliminate the need for external active components and end-user calibration.

The ST200GC is provided in 4x4x1.2mm^3 Quad Flat No-lead (QFN) package.

Applications

- Smartphone
- Tablet
- Handheld devices
- Unmanned Aviation Vehicles

Content

1. Functional Diagram

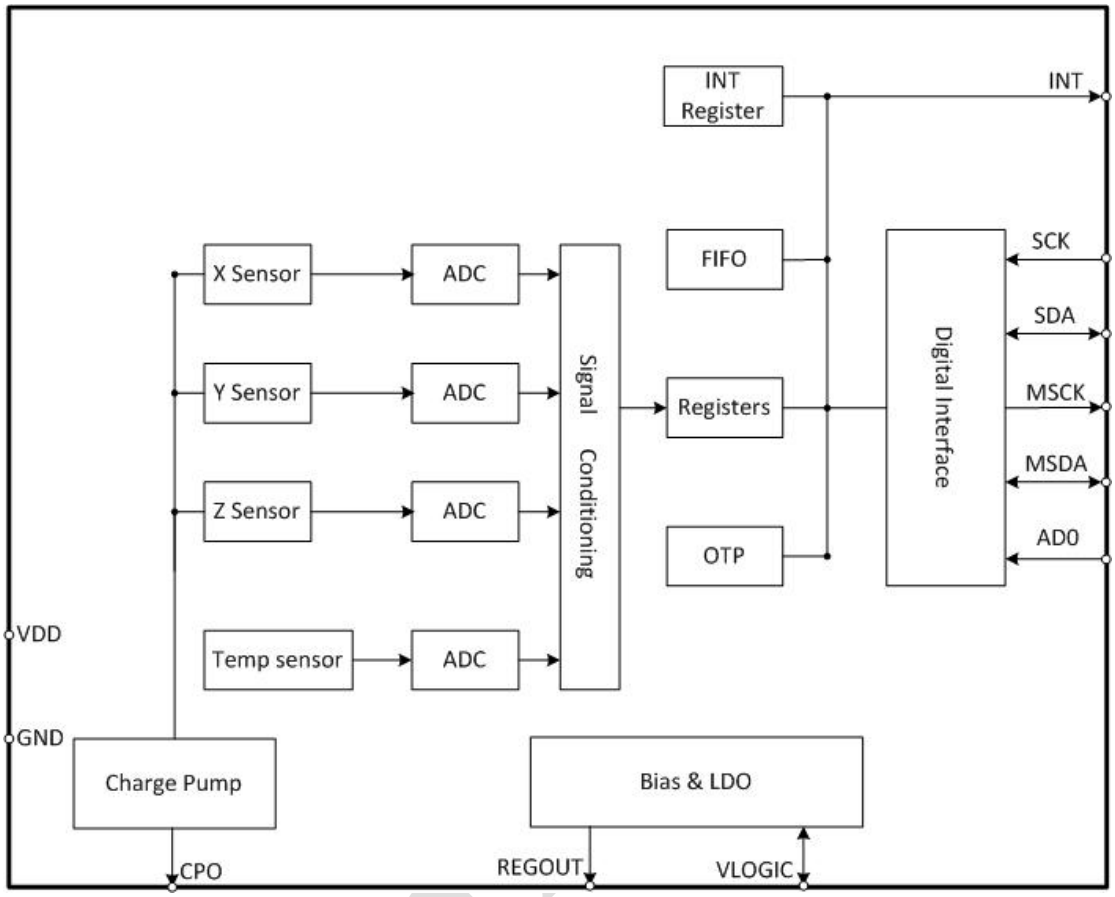


Figure 1. Function Block Diagram

2. Electrical Characteristics

2.1 Gyroscope Sensor Specifications

DC Operating Parameters T=-40℃ to 85℃, Vdd = 2.1V to 5V (unless otherwise specified)

All parameters specified are @ Vdd=3.0V and T=25℃

Parameter	Conditions	Min.	Typ.	Max.	Unit
Full Scale Range			±2000		º/s
Sensitivity			0.512		LSB/ º/s
Sensitivity scale factor tolerance		-6	±2	+6	%
Non-Linearity	25℃ Best Fit Straight Line		±0.2		%FS
Scale Factor Drift	-40℃ ~85℃		±10		%
Cross-sensitivity			±2		%
Zero Rate Output					
Initial ZRO Tolerance			±5		º/s
ZRO Variation Over Temperature	-40℃~85℃		±10		º/s
Total RMS Noise	DLPFCFG select 100Hz		0.5625		º/s-rms
Output Data Rate	Programmable			1,000	Hz
Gyroscope Start-up Time ZRO setting	DLPFCFG=0 to ±1% of final		50		ms

2.2 Electrical and Other Common Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD Power Supply Operating Voltages		2.1	3.3	5	V
Normal Operating Current	Gyroscope		6.1		mA
Full Chip Idle Mode Supply Current			5		uA
Power Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to			100	mS

	90% of the final value				
VLOGIC REFERENCE VOLTAGE Voltage Range Power Supply Ramp Rate Normal Operating Current	VLOGIC must be <VDD at all times Monotonic ramp. Ramp rate is 10% to 90% of the final value	1.71	 100	VDD 2	V mS μA
Start–up Time for Register Read/Write		20		100	mS

Parameter	Conditions	Min.	Typ.	Max.	Unit
Temperature Range	Performance parameters are not applicable beyond specified temperature range	-40		85	℃
Sensitivity	Untrimmed		2		LSB/℃
Temperature Offset	25℃		-1		LSB
Nonlinearity	Best fit straight line(-40℃ to +85℃)		±1		℃
IIC Address	AD0=0 AD0=1		1101000 1101001		
DIGITAL INPUTS(MSDA/SDA, MCLK/SCLK, AD0, CLKIN) V_{IH}, High Level Input Voltage V_{IL}, Low Level Input Voltage C_I, Input Capacitance		0.7*VLOGIC	<5	0.3*VLOGIC	V V pF
DIGITAL OUTPUT(INT) V_{OH}, High Level Output Voltage V_{OL1}, Low Level Output Voltage V_{OL_INT1}, INT Low Level Output Voltage Output Leakage Current t_{INT}, INT Pulse Width	R_{LoAD}=1MΩ OPEN=1,0.3mA sink Current OPEN=1 LATCH_INT_EN=0	0.9*VLOGIC	100 50	0.1*VLOGIC 0.1	V V V nA μs

Parameter	Conditions	Typ.	Unit
PRIMARY IIC I/O (SCL, SDA)			
VIL, Low-Level Input Voltage		-0.5V to 0.3*VLOGIC	V
VIH, High-Level Input Voltage		0.7*VLOGIC to VLOGIC+0.5V	V
Vhys, Hysteresis		0.1*VLOGIC	V
V_{OL1}, Low-Level Output Voltage	3mA sink current	0 to 0.4	V
I_{OL}, Low-Level Output Current	V_{OL}=0.4V	3	mA
	V_{OL}=0.6V	5	mA
Output Leakage Current		100	nA
t_{of}, Output fall time form V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b to 250	ns
C_I, Capacitance for Each I/O pin		<10	pF
Auxiliary IIC I/O (MSCK, MSDA)	AUX_VDDIO=0		
VIL, Low-Level Input Voltage		-0.5V to 0.3*VLOGIC	V
VIH, High-Level Input Voltage		0.7*VLOGIC to VLOGIC+0.5V	V
Vhys, Hysteresis		0.1*VLOGIC	V
V_{OL1}, Low-Level Output Voltage	VLOGIC>2V;1mA sink current	0 to 0.4	V
V_{OL3}, Low-Level Output Voltage	VLOGIC<2V;1mA sink current	0 to 0.2*VLOGIC	V
I_{OL}, Low-Level Output Current	V_{OL}=0.4V	1	mA
	V_{OL}=0.6V	1	mA
Output Leakage Current		100	nA
t_{of}, Output fall time form V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b to 250	ns
C_I, Capacitance for Each I/O pin		<10	pF
Auxiliary IIC I/O (MSCK, MSDA)	AUX_VDDIO=1		
VIL, Low-Level Input Voltage		-0.5V to 0.3*VLOGIC	V
VIH, High-Level Input Voltage		0.7*VLOGIC to VLOGIC+0.5V	V
Vhys, Hysteresis		0.1*VLOGIC	V
V_{OL1}, Low-Level Output Voltage	1mA sink current	0 to 0.4	V
I_{OL}, Low-Level Output Current	V_{OL}=0.4V	1	mA
	V_{OL}=0.6V	1	mA
Output Leakage Current		100	nA
t_{of}, Output fall time form V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b to 250	ns
C_I, Capacitance for Each I/O pin		<10	pF

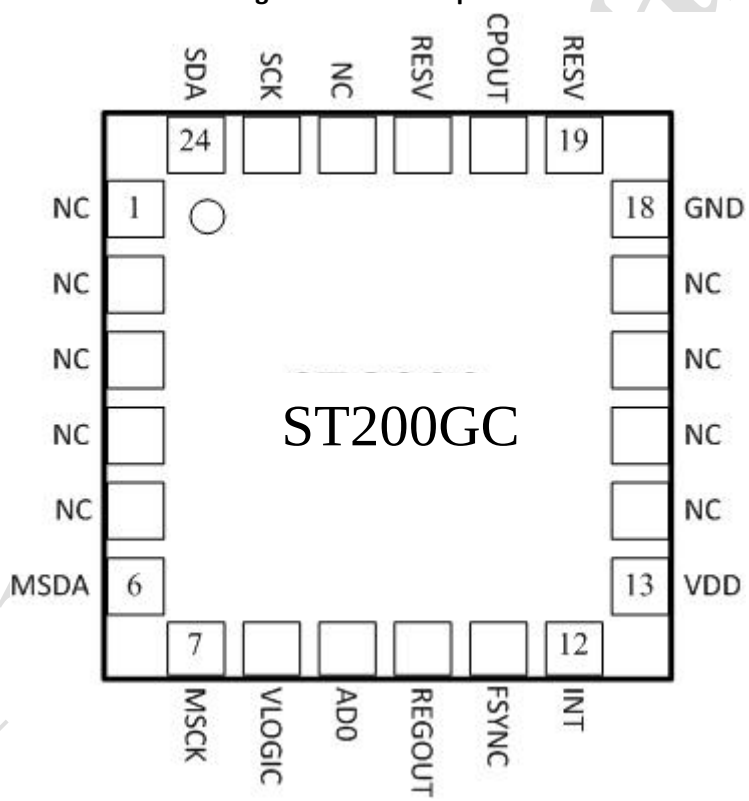
3. Absolute Maximum Rating

Stress above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter	Rating
Operating Supply Voltage	-0.3V ~ 6V
Operating Temperature Range	-40℃ ~ 85℃
Storage Temperature Range	-40℃ ~ 105℃
ESD	2000V (HBM)
Latch up	JEDEC Class II (2), 125℃, Level B, ±60mA

4. Pin Description

Figure 2. Pin Description



(Top View)

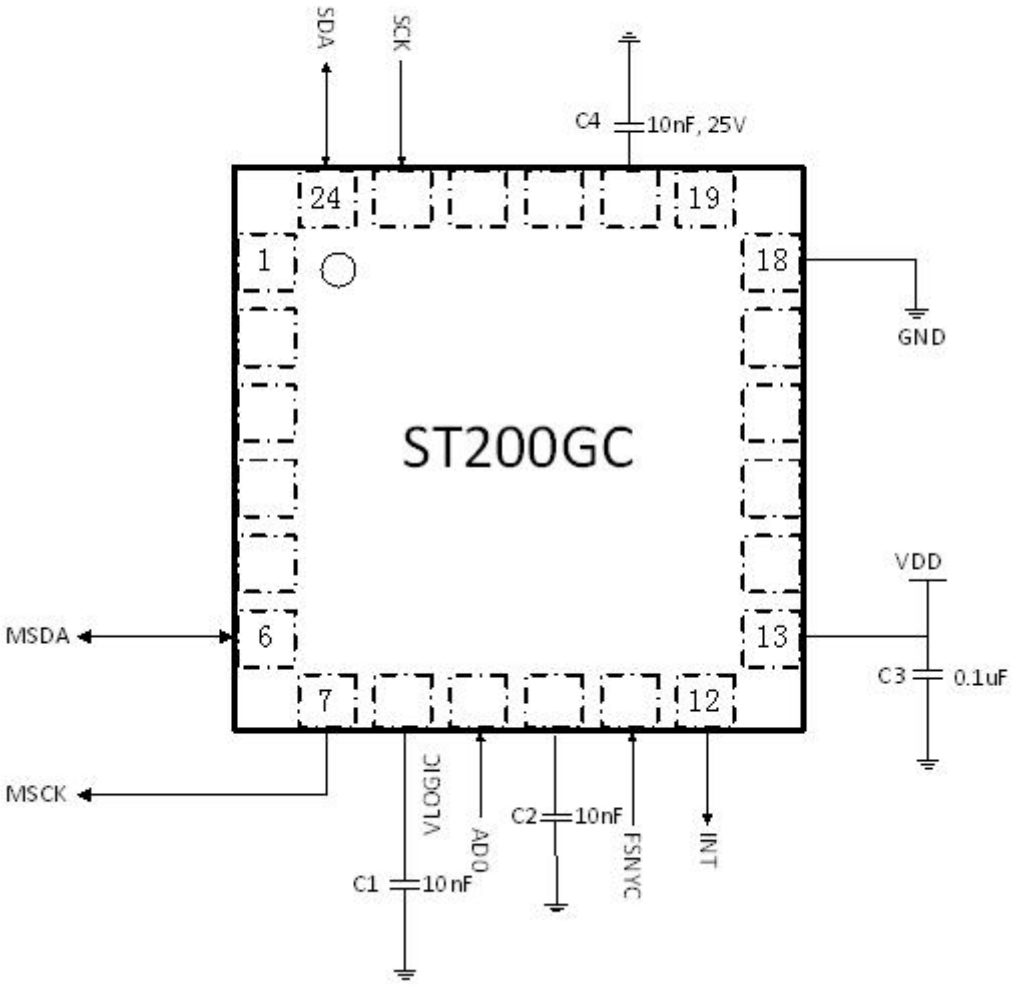
Pin No.	Pin Name	PIN Function
6	MSDA	Auxiliary IIC serial data, for connecting to external sensors
7	MSCK	Auxiliary IIC serial clock, for connecting to external sensors
8	VLOGIC	Digital I/O supply voltage
9	AD0	IIC slave Address LSB (AD0)
10	REGOUT	Regulator filter capacitor connection

11	FSYNC	Synchronization CLK input, connect to GND if not used
12	INT	Interrupt digital output(totem pole or open-drain)
13	VDD	Power supply voltage and Digital supply voltage
18	GND	Power supply ground
19,21	RESV	Reserved. Do no connect
20	CPOUT	Charge pump capacitor connection
23	SCK	IIC serial clock(SCK)
24	SDA	IIC serial data
1,2,3,4,5,14,15,16,17，22	NC	Not internally connected. May be used for PCB trace routing

5. Application Information

5.1 Typical Application Circuit

Figure 3.Reference Application Circuit



5.2 Bill of Materials for External Components

Item	Quantity	Reference	Value	Remarks
1	1	C1	10nF	X7R or X5R Grade
2	1	C2	10nF	X7R or X5R Grade
3	1	C3	0.1uF	X7R or X5R Grade
4	1	C4	10nF	X7R or X5R Grade, 25V

5.3 Overview

The ST200GC is comprised of the several key blocks and functions:

- Tri-axis MEMS angular rate sensor with 11-bit ADCs and signal conditioning
- Digital signal processor
- Primary IIC interface
- Auxiliary IIC interface
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO
- Charge Pump

5.3.1 Tri–axis MEMS Sensor with 11-bit ADCs and Signal Conditioning

The ST200GC consists of three independent angular rate sensors. It detects rotation on the X, Y and Z axes. When the gyro is rotated around any of these sense axes, the movement caused by Coriolis Effect will be detected. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. For each axis an on-chip 11-bit ADC is used to digitize the output voltage. The full-range of the gyroscope is ±2000º/s.

5.3.2 Primary IIC Communications Interfaces

The ST200GC communicates to a system processor via IIC serial interface, and the device always acts as a slave when communicating to the system processor. The LSB of the IIC slave address is set by Pin 9 (AD0).

5.3.3 Auxiliary IIC Serial Interface

The ST200GC has an auxiliary IIC bus which allows an external system processor to act as master and directly communicate to the external accelerometer connected to the secondary I2C bus pins (MSDA and MSCK). This is useful for configuring the accelerometers, or for keeping the ST200GC in a low-power mode, when only accelerometers are to be used. In this mode, the secondary I2C bus control logic (third-party accelerometer Interface block) of the ST200GC is disabled, and the secondary I2C pins MSDA and MSCK are connected to the main I2C bus through analog switches.

The diagram below shows an application processor can communicate to the digital output sensor connected to ST200GC through the Auxiliary IIC bus.

5.3.4 FIFO

The ST200GC contains an embedded memory management system of 32-level FIFO that can be

used to relieve host processor burden. It has four modes:

Bypass Mode: In Bypass mode, FIFO is not operational and it remains empty.

FIFO Mode: Data from measurements of the x-, y- and z- axis are stored in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFOConf register, the watermark interrupt bit is set. FIFO continues to accumulate data until it is full and then stops collecting data. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the sample bits of the FIFOConf register.

Stream Mode: Data from measurements of the x-, y- and z-axis are store in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFOConf register, the watermark interrupt bit is set. FIFO continues accumulating samples and holds the latest 32 samples from measurements of x-, y- and z- axis, discarding older data as new data arrives; The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the sample bits of the FIFOConf register.

Trigger Mode: In Trigger mode, FIFO accumulates samples, holding the latest 32 samples from measurements of the x-, y- and z- axis. After a trigger event occurs and an interrupt is sent, FIFO keeps the last n samples (where n is the value specified by the samples bits in the FIFOConf register) and then operates in FIFO mode, collecting new samples only when FIFO is not full.

Note that the FIFO data should be read first because placing the device into bypass mode clears FIFO.

5.3.5 Bias and LDO

The bias and LDO circuitry provide the internal supply, the reference voltages and currents required by the whole chip. Its two inputs include an unregulated VDD of 2.1V to 3.6V and a logic reference supply voltage from 1.71V to VDD.

5.3.6 Charge Pump

An on-chip charge pump generates the high voltage required for the MEMS oscillation. Its output is bypassed by a capacitor at Pin20 (CPOUT).

6. Register Map and Description

The register map of ST200GC is listed below:

Reg No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20	0x82	Sensor_da	R	Sensor data read command							

		ta										
33	R:0xC1 W:0xA1	Aux_ctl	R/W	Reserved					Aux_en	Reserved		
64	R:0xE0 W:0x60	IntrSta	R	DataRdy	Reserved						Watermark	Reserved
65	R:0xE1 W:0x61	FifoSta	R	full	empty	Fifo level						
71	R:0xE7 W:0x67	FifoConf	R/W	FifoMode		Samples						
72	R:0xE8 W:0x68	IntrConf	R/W	IntrMode					Reserved			
73	R:0xE9 W:0x69	IntrEnConf	R/W	DataRdy	Reserved						Watermark	Reserved
86	R:0X16 W: 0X76	Pwr_ctrl	R/W	Sleep	Reserved							
90	R:0x1A W:0x7A	Filt_conf	R/W	Reserved				Tempflt_en	Hpf_bp	Odr_conf		Filt_en
93	R:0X1D W: 0X7D	PLL_conf		Reserved				PLL_en	Reserved			

6.1 Register 20–Sensor Data Read Command

Type: Read Only

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
20	0x82	Sensor_data	R	Sensor data read command								8'h00

Description:

A read command to address 0x82 will return 6 bytes consecutive sensor data including X/Y/Z axis. The data of each sensor axis contain 2 bytes.

Parameter:

Table of each axis sensor data assignment:

Byte No.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

1	Gyro_Xout[2:0]	Reserved
2	Gyro_Xout[10:3]	
3	Gyro_Yout[2:0]	Reserved
4	Gyro_Yout[10:3]	
5	Gyro_Zout[2:0]	Reserved
6	Gyro_Zout[10:3]	

6.2 Register 33–Auxiliary IIC control

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
33	R:0XC1 W:0xA1	Aux_ctl	R/W	Reserved				Aux_en	Reserved			8'h00

Type: Read/Write

Description:

This register controls the auxiliary IIC pass through mode.

Parameter:

BIT	SYMBOL	DESCRIPTION
7:1		Reserved
3	Aux_en	1'b0 : disable the auxiliary IIC pass through mode. 1'b1 : enable the auxiliary IIC pass through mode.
2:0		Reserved

6.3 Register 64–Interrupt Status

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
64	R:0XE0 W:0x60	IntrSta	R	DataRdy	Reserved					Watermark	Reserved	8'h00

Type: Read only

Description:

This register is used to determine the status of ST200GC interrupt. When an interrupt is triggered, corresponding bit will be set. Check the interrupt status bits will tell what kind of interrupt has been triggered.

Parameter:

BIT	SYMBOL	DESCRIPTION
7	DataRdy	1'b0 : no new sensor data 1'b1 : new sensor data is ready
6:2		Reserved
1	Watermark	1'b1: FIFO watermark is reached 1'b0: FIFO watermark is not reached
0		Reserved

6.4 Register 65–Interrupt Status

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
64	R:0XE1 W:0x61	FifoSta	R	full	empty	Number of FIFO entry						8'h00

Type: Read only

Description:

This register is used to determine the status of FIFO.

Parameter:

BIT	SYMBOL	DESCRIPTION
7	full	1'b0 : FIFO is not full 1'b1 : FIFO is full
6	empty	1'b1: FIFO is empty 1'b0: FIFO is not empty
5:0	Watermark	Number of FIFO entries hold data

6.5 Register 71–Fifo configuration

Type: Read/Write

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
71	R:0XE7 W:0x67	FifoConf	R/W	FifoMode		Samples						8'h00

Description:

This register configures FIFO mode and FIFO watermark. Four FIFO modes are supported. Watermark level is set and when it is reached, an interrupt status will be set to inform the processor to start to read FIFO to avoid FIFO overflow.

Parameter:

BIT	SYMBOL	DESCRIPTION
7:6	Fifo_mode	2'b00 : bypass. 2'b01 : fifo. 2'b10 : stream. 2'b11: trigger.
5:0	Samples	Watermark level Maximum value is 6'h20 for 32-level

6.6 Register 72– Interrupt mode configuration

Type: Read/Write

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
72	R:0xE8 W:0x68	IntrConf	R/W	IntrMode				Reserved				8'h00

Description:

Interrupt pin can be configured to show desired electrical behavior. The interrupt pin output type can be set either as push-pull or as open drain. Also interrupt status clear method can be set.

Parameter:

BIT	SYMBOL	DESCRIPTION
7		0: INT output is high. 1: INT output is low.
6		0:normal output PAD. 1:open-drain output PAD.
5		0:output is level. 1:output is pulse.
4	Int_clr	1:random read clear. 0:readint status register clear.
3:0		reserved

6.7 Register 73 – Interrupt configuration

Type: Read/Write

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
73	R:0xE9	IntrEnConf	R/	Data	Reserved					Water	reser	8'h00

	W:0x69		W	Rdy		mark	ved	

Description:

Data ready, FIFO watermark reached or master IIC error Interrupt can be enabled by setting corresponding bit of this register.

Parameter:

BIT	SYMBOL	DESCRIPTION
7	DataRdy	1: DataRdyint enable. 0: DataRdyint disable.
6:2		Reserved
1	watermark	1: watermark int enable. 0: watermark int disable.
0		Reserved

6.8 Register 86 – Power Control

Type: Read/Write

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
86	R:0x16 W:0x76	Pwr_ctrl	R/W	Sleep	Reserved							8'h00

Description:

This register is used to manage the power control. Setting the Sleep bit in the register will put the chip under low power sleep mode and only IIC serial interface remains active.

Parameter:

BIT	SYMBOL	DESCRIPTION
7	Sleep	1: enable low power sleep mode 0: normal operation mode
6:0		Reserved

6.9 Register 90-Digital Filter Configuration

Type: Read/Write

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
90	R:0x1A W:0x7A	Filt_conf	R/W	Reserved			Tempflt_en	Hpf_bp	Odr_conf		Filt_en	8'h00

Description:

This register controls the ODR and digital filters. Digital filter must be enabled in order to read data from IIC bus.

Parameter:

BIT	SYMBOL	DESCRIPTION
7:5	rev	Reserved
4	Temp filt_en	1: Temperature low pass filter enable 0: Temperature low pass filter disable
3	hpf_bp	1: bypass digital high pass filter 0: doesn't bypass digital high pass filter
2:1	odr_conf	Output data rate select: 2'b00 : 1000 Hz 2'b01 : 500 Hz 2'b10 : 250 Hz 2'b11 : 31.125 Hz
0	filt_en	1: digital filter enable 0: digital filter disable

6.10 Register 93-PLL Configuration

Type: Read/Write

Reg. No.	Addr (Hex)	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
93	R:0x1D W:0x7D	PLL_conf	R/W	Reserved			PLL_en	Reserved				8'h00

Description:

This register controls to switch between PLL and oscillator as internal clock source. PLL is strongly recommended in order to get better performance.

Parameter:

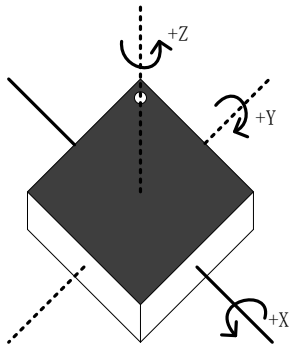
BIT	SYMBOL	DESCRIPTION
7:5		Reserved
4	PLL_en	1: enable PLL for better performance 0: use oscillator as clock source, not recommended
3:0		Reserved

7. Package Dimensions:

ST200GC is provided in Quad Flat No-lead (QFN) package and RoHS compliant. The size is: 4x4x1.2mm^3.

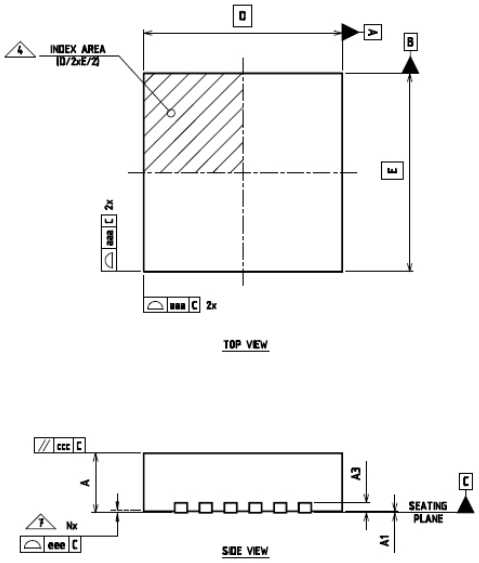
7.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 marker in the figure.

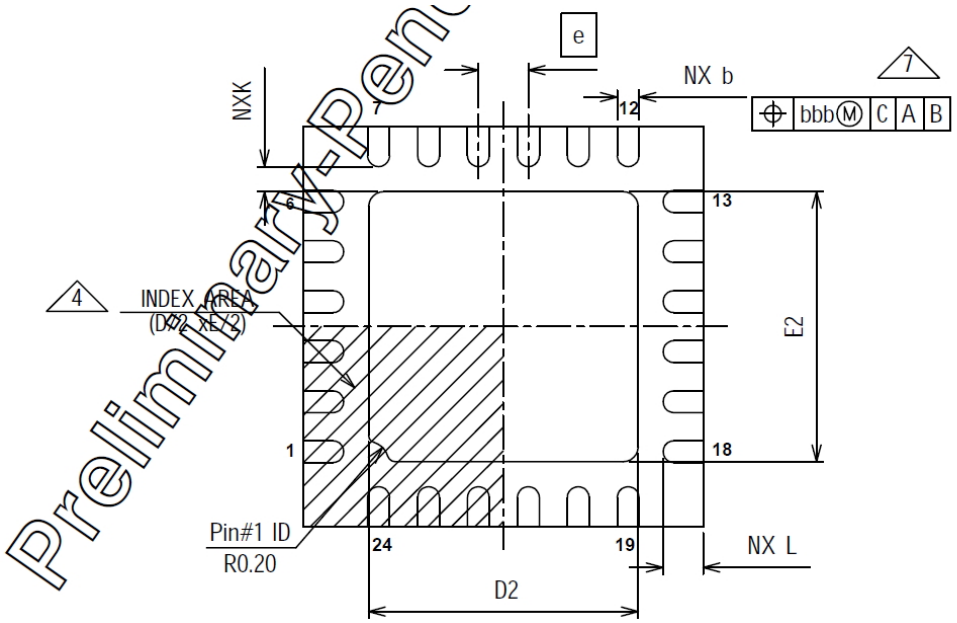


Orientation of Axes Sensitivity and Polarity of Rotation

7.2 Package Dimensions:



Dimension Table				
Thickness / Symbol	1.20			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	1.15	1.20	1.25	
A1	0.00	0.02	0.05	
A3	---	0.203 Ref	---	
b	0.18	0.25	0.30	6
L	0.25	0.35	0.45	
D	4.00 BSC			
E	4.00 BSC			
e	0.50 BSC			
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	24			3
ND	6			5
NE	6			5
NOTES	1, 2			
LF DWG NO.	B-3572			
REV.	2			



Note: The exposed die pad is not connected to any circuit or power/ground inside the chip. Neither is the die pad required for heat sinking. Hence the die pad should not be soldered to the PCB.

8. Revision History

Date	Revision	Changes
2015-06-10	Reversion 1.4	Preliminary version.

9. Disclaimer

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